REMARKS

Claims 1-16 and 18-58 are present in this application. Claims 16, 18-38, and 58 have been examined. Claims 16, 28, and 37 are independent claims.

Allowable Subject Matter

Independent claims 28 and 37 are allowed, and dependent claim 22 is allowable, if re-written into independent form.

Statement of Substance of the Interview, MPEP 713.04

A telephone interview was conducted on April 16, 2008, in order to clarify the Examiner's position with regard to the claimed "such that a surface of the non-single-crystal silicon thin-film that is nearest to the insulating substrate and a surface of the single-crystal silicon thin-film that is nearest to the insulating substrate are at different heights above the insulating substrate."

The Examiner stated that it was her position that gate electrode 307, which is polycrystalline, is at a different height than the single-crystal silicon thin-film 302 in Drawing 4.

Applicants have amended claim 16 to include that the non-single-crystal thin-film whose surface is nearest to the insulating substrate is the first non-single-crystal silicon thin-film layer above the insulating substrate.

§ 102(b) Rejection – Yudasaka

Claims 16, 18-21, 23, 24, 29-34, and 58 have been rejected under 35U.S.C. § 102(b) as being anticipated by JP 06-011729 (Yudasaka). Applicants respectfully traverse this rejection.

Summary of the Claimed Invention

Embodiments of the present invention are directed to a semiconductor device, comprising a non-single-crystal thin-film device and a single-crystal silicon thin-film device, wherein the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device are provided in different areas of an insulating substrate (specification at page 33).

The non-single-crystal silicon thin-film device is manufactured from a non-single-crystal silicon thin film, and the single-crystal silicon thin-film device is manufactured from a single-crystal silicon thin film. The non-single-crystal silicon thin-film and the single-crystal silicon thin-film are each separated from the insulating substrate by a space, or at least one other layer. In an example embodiment, a single-crystal silicon substrate 10a is formed to include a protective insulating film and planarized film (BPSG), which is mounted to the insulating substrate (specification at pages 41-42). The single-crystal silicon thin film 14a remaining after cleavage stripping (Fig. 1(c)) is prevented from contamination and damage to the crystalline structure. The non-single-crystal thin film is formed over a second insulating film 4 (Figs. 1(d) to 1(f)). The resulting structure is such that a surface of the non-single-crystal silicon thin-film that is nearest to the insulating substrate and a surface of the single-crystal silicon thin-film that is nearest to the insulating substrate are at different heights above the insulating substrate (e.g., Fig. 1(i)).

Yudasaka

Yudasaka discloses a structure to drive an active matrix on a single crystal silicon film. Single crystal silicon films 202, 203 provide a peripheral circuit to drive an active matrix formed on an insulating substrate 201. Polycrystalline silicon film or noncrystalline silicon film 204 forms picture element transistors. The single crystal silicon film 202, 203 have thickness larger than the thickness of the polycrystalline silicon film or noncrystalline silicon film 204. (Abstract). In an example embodiment, the thickness of the single crystal silicon films 202 and 203 are 5000A or more, and thickness of the polycrystalline silicon film or the amorphous silicon film 204 is made 1000A or less (para. 0016).

Yudasaka discloses a thin film transistor that is formed on either a silicon on insulator (SOI) substrate or a silicon on sapphire substrate (SOS). Drawing 1 is an example of the SOS

substrate, and shows a single crystal silicon film 102 formed on a transparent insulating substrate 101. (para. 0012, 0013).

Yudasaka discloses forming a single crystal silicon film 302 on a transparent insulating substrate 301, and depositing a polycrystalline silicon film or amorphous silicon film 303 by LPCVD. (Drawing 3 and para. 0017).

Differences over Yudasaka

The Office Action alleges that Yudasaka's single crystal silicon film 302, polycrystalline silicon film or amorphous silicon film 303, and insulating substrate 301 constitute respective claimed features.

Applicants submit that Yudasaka fails to teach the non-single-crystal silicon thin-film 303 and the single-crystal silicon thin-film 302 are each separated from the insulating substrate 301 by a space or at least one other layer.

As noted above, both the non-single-crystal silicon thin-film 303 and the single-crystal silicon thin-film 302 in Yudasaka are each formed on the transparent insulating substrate 301. Yuasaka does not disclose a space or one other layer separating the respective thin films from the insulating substrate 301.

In further arguments, the Examiner states that "layers 202 and 302 are deposited on the SOS substrate and therefore are separated from substrate layer 101 by layer 102." (Response to Arguments). Applicants submit that this argument is in error.

Layer 102 is disclosed as being the single crystal silicon film 102 formed on the transparent insulating substrate 101 (para. 0013). According to para. 0015: "on the transparent insulating substrate 201, the single crystal silicon films 202 and 203 with which a circumference circuit is prepared are formed."). Thus, Applicants submit that layer 102, the single crystal silicon film, is formed to become single crystal silicon films 202, 203.

The Examiner also states that in the case of an SOI substrate, the insulator would constitute an inherent layer formed between the substrate and the silicon layer. Applicants disagree.

Applicants submit that an SOI substrate is by definition a type of substrate having an embedded insulation layer. Yudasaka does not disclose a layer between the SOI substrate (i.e. the insulating substrate) and the respective silicon films.

Claim 16 requires "the non-single-crystal silicon thin-film and the single-crystal silicon thin-film are each separated from the insulating substrate by a space or at least one other layer."

The resulting structure of a semiconductor device of the present invention is such that a surface of the non-single-crystal silicon thin-film that is nearest to the insulating substrate and a surface of the single-crystal silicon thin-film that is nearest to the insulating substrate are at different heights above the insulating substrate.

During a telephone interview, the Examiner expressed that because gate electrode is made of polycrystalline silicon (para. 0021), then gate electrode 307 can be considered as the claimed non-single-crystal silicon thin-film, thereby meeting the claimed feature. In order to avoid this unintentional interpretation, Applicants have amended claim 16 to state: "wherein the non-single-crystal silicon thin-film is the first non-single-crystal silicon thin-film layer above the insulation substrate." Applicants submit that silicon film 303, which is the first non-single-crystal silicon thin-film layer above the insulation substrate 301, is formed on the insulation substrate 301 along with the single crystalline silicon film 302, i.e. the same height.

For at least these reasons, Applicants submit that Yudasaka fails to teach each and every feature of claim 16.

Further with respect to claim 21, Applicant submits that Yudasaka explicitly teaches that the thickness of the single crystal silicon film is 5000A or more (i.e. 500 nm or more; para. 0016). The Examiner appears to allege that the thickness of 5000A is for the combination of silicon films 202 and 203. Applicants disagree. In any case, since both silicon films are formed from the same single-crystalline film 102, according to the Examiner's interpretation the thickness of each silicon film 202,203 would be 2500A. Furthermore, Yudasaka requires that the single crystal silicon film 202, 203 have thickness larger than the thickness of the polycrystalline

silicon film or noncrystalline silicon film 204 (Abstract). Thus, it can be seen that Yudasaka teaches that the thickness of the single crystal silicon film 202, 203 must be greater than 100 nm.

On the other hand, Claim 21 requires a thickness of about not more than 100 nm.

For at least this additional reason, Applicant submits that Yudasaka fails to teach at least the features of claim 21.

Further with respect to claim 58, Applicants submit that one of ordinary skill would understand that the claimed intervening inorganic insulating film for bonding the single-crystal thin-film device to the insulating substrate is not an insulating film embedded in the insulating substrate. Applicants submit that Yudasaka fails to teach an intervening insulating film for bonding the single-crystal thin-film device to an SOI substrate.

For at least this additional reason, Applicant submits that Yudasaka fails to teach at least the features of claim 58.

Applicants request that the rejection be reconsidered and withdrawn.

§ 103(a) Rejection – Yudasaka, Spitzer

Claims 25-27 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yudasaka in view of Spitzer (previously applied). Applicants respectfully traverse this rejection.

Claims 25-27 are dependent claims, indirectly dependent on claim 16. Applicants submit that Spitzer fails to make up for the above stated deficiencies in claim 16. Thus, Applicants submit that at least for the reasons above for claim 16, the rejection fails to establish *prima facie* obviousness for claims 25-27, as well.

§ 103(a) Rejection – Yudasaka, Okabe

Claims 35 and 36 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yudasaka in view of U.S. Patent 5,663,099 (Okabe; previously applied). Applicants respectfully traverse this rejection.

Claims 35 and 36 are dependent claims on claim 16. Applicants submit that Okabe fails to make up for the above stated deficiencies in claim 16. Thus, Applicants submit that at least for the reasons above for claim 16, the rejection fails to establish *prima facie* obviousness for claims 35 and 36, as well.

Conclusion

In view of the above amendment, applicant believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Robert Downs Reg. No. 48,222 at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§1.16 or 1.147; particularly, extension of time fees.

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Respectfully submitted,

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